GF28: SSTL_15

Libraries

Name	Process	Form Factor
RGO_GF28_18V15_SLP_20C_SSTL_15	SLP	staggered
RGO_GF28_18V15_HPP_20C_SSTL_15	HPP	staggered

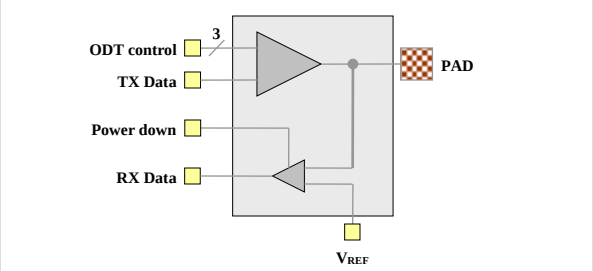
Summary

The SSTL_15 pad set is a full complement of I/O, calibration, power, and spacer cells that are necessary to assemble a padring by abutment. Since the SSTL_15 normally operates with its own isolated power domain (1.5V), a "rail-splitter" support cell (SPP_RS_005_15V) is included to allow the designer to easily break the lines that should not connect to the rest of the padring, while allowing VDD and VSS to be continuous within the padring.

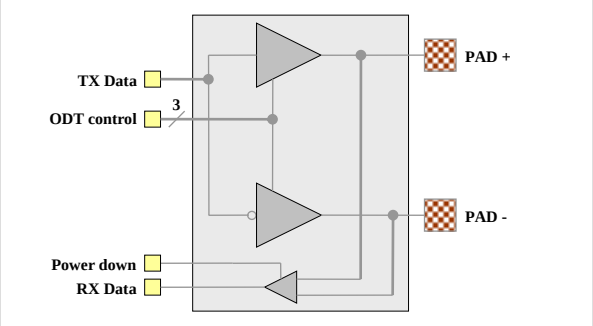
Features

- Full DDR3 capability - 800MHz (1600 Mbps)
- Low Power driving standard DDR3 memories
- 1.8V FETs
- Full complement of cells to build padring (20)
- Full ODT Capability:
  - Either fixed 6-Bit programmation (program from core)
  - Or, dynamic 6-Bit PVT calibration (external reference resistor)

SLP_BI_SDS_15V_D – SSTL_15 Driver



SLP_CL_SDS_15V_D – SSTL_15 Clock Driver



Absolute maximum ratings

Parameter	Description	Value	Units
V_{VDD}	Core supply voltage range	-0.5 to 1.4	V
V_{DVDD}	I/O supply voltage range	-0.5 to 2.1	V
V_{PAD}	Voltage range at PAD	-0.5 to (V_{DVDD} + 0.5)	V

Recommended operating conditions

Parameter	Description		Min	Nom	Max	Units
V_{VDD}	Core supply voltage	SLP	0.9	1.0-	1.1	V
			0.99	1.1	1.155	V
		HPP	0.765	0.85	0.935	V
			0.81	0.9	0.945	V
V_{DVDD}	I/O supply voltage		1.425	1.5	1.575	V
V_{VREF}	Reference voltage		0.49*DVDD	DVDD / 2	0.51*DVDD	V
T_J	Junction temperature		-40	25	125	°C
V_{PAD}	Voltage at PAD		0		V_{DVDD}	V
$V_{IH\ (dc)}$	DC input logic high		V_{REF} + 0.1		TBD	V
$V_{IL\ (dc)}$	DC input logic low		TBD		V_{REF} - 0.1	V
$V_{IH\ (ac)}$	AC input logic high		V_{REF} + 0.175		-	V
$V_{IL\ (ac)}$	AC input logic low		-		V_{REF} - 0.175	V

AC Characteristics

Symbol	Parameter		Max	Unit
F	Max frequency		800	MHz
P_{DISS}(TX)	Power dissipation	100 MHz	10.3	mW
		400 MHz	12.7	mW
		800 MHz	15.8	mW

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Characterization Corners

Nominal VDD	Model	VDD	DVDD= 1.5V	Temperature
1.1 (SLP)	FF	+5%	+10%	-40°C
	FF	+5%	+10%	125°C
	TT	nominal	nominal	25°C
	SS	-10%	-10%	-40°C
	SS	-10%	-10%	125°C
1.0 (SLP)	FF	+10%	+10%	-40°C
	FF	+10%	+10%	125°C
	TT	nominal	nominal	25°C
	SS	-10%	-10%	-40°C
	SS	-10%	-10%	125°C
0.9 (HPP)	FF	+5%	+10%	-40°C
	FF	+5%	+10%	125°C
	TT	nominal	nominal	25°C
	SS	-10%	-10%	-40°C
	SS	-10%	-10%	125°C
0.85 (HPP)	FF	+10%	+10%	-40°C
	FF	+10%	+10%	125°C
	TT	nominal	nominal	25°C
	SS	-10%	-10%	-40°C
	SS	-10%	-10%	125°C

Physical sizes

Name	Width	Height	Units
SLP_BI_SDS_15V_D/DVDD/DVSS/PDO	40	150	µm
SLP_CL_SDS_15V_D_PWR	80	150	µm
SLP_SP_CAL_SDS_15V	35	150	µm
SLP_RE_000_15V	20	150	µm
PVP_VD_RCD_1015V	20	150	µm
PVP_VS_RCD_1015V	20	150	µm
SVP_SP_000_15V	0.1	150	µm
SVP_SP_001_15V	1	150	µm
SVP_SP_005_15V	5	150	µm
SVP_SP_020_15V	20	150	µm
SPP_RS_005_15V	5	150	µm
SPP_AD_SSTL_15V	20	150	µm
SVP_CO_001_15V	150	150	µm

Cell summary

Name	Description
SLP_BI_SDS_15V_D /DVDD/DVSS/PDO	SSTL_15 I/O pad with power
SLP_CL_SDS_15V_D_PWR	Differential clock buffer with DVDD/DVSS
SLP_SP_CAL_SDS_15V	Calibration pad
SLP_RE_000_15V	V_{REF} pad
PVP_VD_RCD_1215V	Core V_{DD} with VREF bus
PVP_VS_RCD_1215V	Core V_{SS} pad with VREF bus
SVP_SP_000_15V	0.1 µm spacer
SVP_SP_001_15V	1 µm spacer
SVP_SP_005_15V	5 µm spacer
SVP_SP_020_15V	20 µm spacer
SPP_RS_005_15V	DVDD, DVSS, POC, CP[1..3], CN[1..3] and VREF rail splitter
SPP_AD_SSTL_15V	Adapter to staggered libraries
SVP_CO_001_15V	Corner cell

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