TSMC 06/07: 1.8V 100MHz Oscillator

Libraries

Name	Process	Form Factor
RGO_TSMC06_18V18_6FF_20F_OSC	6FF	Staggered Flip Chip
RGO_TSMC07_18V18_7FF_20C_OSC	7FF	Staggered Flip Chip

Summary

The 1.8V 100MHz Oscillator library provides high gain / low power crystal oscillator macro I/O cells capable of operation over a wide frequency range.

This library is offered at both 6nm and 7nm. It is available in a staggered flip chip implementation.

To design an operational I/O power domain with these cells, an additional library is required – 1.8V Support: Power. That library contains an input-only buffer, isolated analog I/O, and a full complement of power cells along with corner and spacer cells to assemble a functional pad ring by abutment. An included rail splitter allows multiple power domains to be isolated in the same pad ring while maintaining continuous VDD/VSS for robust ESD protection.

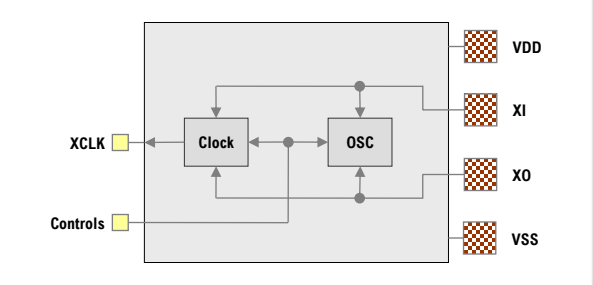
ESD Protection:

- JEDEC compliant
  - 2kV ESD Human Body Model (HBM)
  - 500 V ESD Charge Device Model (CDM)

Latch-up Immunity:

- JEDEC compliant
  - Tested to I-Test criteria of ± 100mA @ 125°C

OSP_BI_100_18V



100 MHz Oscillator Features

- Wide frequency range – 1 MHz to 100 MHz
- Low self-noise – optimized for stability and minimum jitter
- Characterized with industry-standard external crystals
- Power-down mode
- Bypass operating modes
  - BYP18 – XI can be driven by a 1.8V external clock
  - Forced bypass – XI can be driven by a core-level (VDD) clock signal with oscillator normally enabled
- Operates on core power only (VDD/VSS cells embedded)

Cell Size & Form Factor

- Staggered (pad-limited) – 68.16µm x 191.28µm
- Flip chip implementation with CUP structure built in

Recommended Operating Conditions

	Description		Min	Nom	Max	Units
V_{VDD}	Core supply voltage		0.675	0.75	0.825	V
V_{DVDD}	I/O supply voltage		1.62	1.8	1.98	V
			1.35	1.5	1.65	V
			1.08	1.2	1.32	V
T_J	Junction temperature		-40	25	125	°C
V_{PAD}	Voltage at XI	N / F [1]	0	-	V_{VDD}	V
		BYP18 [2]	0	-	1.98	V

[1] XI can be driven by an external clock in Normal operating mode (Forced bypass).
[2} In BYP18 mode, XI can be driven by a 1.8V external clock.
XO should never be driven or loaded by anything other than the crystal.

Characterization Corners

Model [1]	LPE Type	VDD=0.75V	DVDD [2]	Temp
FF	Cbest_CCbest	+10%	+10%	-40°C
FF	Cbest_CCbest	+10%	+10%	0°C
FF	Cbest_CCbest	+10%	+10%	125°C
FFG	Ctypical	+10%	+10%	125°C
TT	Ctypical	nominal	nominal	25°C
TT	Ctypical	nominal	nominal	85°C
SS	Cworst_CCworst	-10%	-10%	-40°C
SS	Cworst_CCworst	-10%	-10%	0°C
SS	Cworst_CCworst	-10%	-10%	125°C

[1] Listed models are for 7FF. 6FF models are FFGNP / TT / SSGNP.
[2] DVDD = 1.8V, 1.5V & 1.2V

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