

TSMC 06/07: 1.8V Support: Power



Libraries

Name	Process	Form Factor
RGO_TSMC06_18V18_6FF_20F_SPT	6FF	Staggered Flip Chip
RGO_TSMC07_18V18_7FF_20C_SPT	7FF	Staggered Flip Chip

Summary

The 1.8V Support: Power library provides a full complement of cells to support the assembly of a functional pad ring by abutment. It is supplied as a standard addition to the GPIO libraries and other I/O library offerings from Aragio Solutions that use a compatible pad ring bus structure.

This library is offered at both 6nm and 7nm. It is available in a staggered flip chip implementation.

The included rail splitter allows multiple power domains to be isolated in the same pad ring while maintaining continuous VDD/VSS for robust ESD protection.

ESD Protection:

- JEDEC compliant
 - 2kV ESD Human Body Model (HBM)
 - 500 V ESD Charge Device Model (CDM)

Latch-up Immunity:

- JEDEC compliant
 - Tested to I-Test criteria of $\pm 100\text{mA}$ @ 125°C

Cell Size & Form Factor

- Staggered (pad-limited) – $17.04\mu\text{m} \times 214.68\mu\text{m}$
- Flip chip implementation with CUP structure built in

Recommended Operating Conditions

Description	Min	Nom	Max	Units
V _{VDD} Core supply voltage	0.675	0.75	0.825	V
	1.62	1.8	1.98	V
V _{DVDD} I/O supply voltage	1.35	1.5	1.65	V
	1.08	1.2	1.32	V
T _J Junction temperature	-40	25	125	°C
V _{PAD} Voltage at PAD	V _{DVSS} -0.3	-	V _{DVDD} +0.3	V

Cell List

Name	Description
Digital Pads	
STP_IN_001_18V_NC	Input-only buffer
I/O Power / Ground Pads	
PWP_VD_PDO_18V	I/O power (DVDD) with POC
PWP_VD_RDO_18V	I/O power (DVDD)
PWP_VS_RDO_18V	I/O ground (DVSS)
Core Power / Ground Pads	
PWP_VD_RCD_10V	Core power (VDD)
PWP_VS_RCD_10V	Core ground (VSS)
Analog Pads *	
ANP_BI_DWR_18V	Isolated analog input cell
Analog Power / Ground Pads	
PWP_VD_ANA_10V	Analog power (AVDD) 0.8V
PWP_VS_ANA_10V	Analog ground (AVSS)
PWP_VD_ANA_18V	Analog power (ADVDD) 1.8V
PWP_VS_ANA_18V	Analog ground (ADVSS)
Support Pads	
SPP_CO_000_18V	Corner cell (rail splitter)
SPP_CO_001_18V	Corner cell (continuous)
SPP_SP_000_18V	0.1 μm spacer
SPP_SP_001_18V	1 μm spacer
SPP_SP_005_18V	5 μm spacer
SPP_SP_010_18V	10 μm spacer
SPP_RS_005_18V	Rail splitter

Characterization Corners

Model [1]	LPE Type	VDD=0.75V	DVDD [2]	Temp
FF	Cbest_CCbest	+10%	+10%	-40°C
FF	Cbest_CCbest	+10%	+10%	0°C
FF	Cbest_CCbest	+10%	+10%	125°C
FFG	Ctypical	+10%	+10%	125°C
TT	Ctypical	nominal	nominal	25°C
TT	Ctypical	nominal	nominal	85°C
SS	Cworst_CCworst	-10%	-10%	-40°C
SS	Cworst_CCworst	-10%	-10%	0°C
SS	Cworst_CCworst	-10%	-10%	125°C

[1] Listed models are for 7FF. 6FF models are FFGNP / TT / SSGNP.
 [2] DVDD = 1.8V, 1.5V & 1.2V

© 2011-2022 Aragio Solutions. All rights reserved.

Information in this document is subject to change without notice. Aragio Solutions may have patents, patent applications, trademarks, copyrights or other intellectual property rights covering subject matter in this document. Except as expressly provided in any written license agreement from Aragio, the furnishing of this document does not give you any license to the patents, trademarks, copyrights, or other intellectual property.

Published by:

Aragio Solutions
2201 K Avenue
Section B Suite 200
Plano, TX 75074-5918
Phone: (972) 516-0999
Fax: (972) 516-0998
Web: <http://www.aragio.com/>

While every precaution has been taken in the preparation of this book, the publisher assumes no responsibility for errors or omissions, or for damages resulting from the use of the information contained herein. This document may be reproduced and distributed in whole, in any medium, physical or electronic, under the terms of a license or nondisclosure agreement with Aragio.

Printed in the United States of America