TSMC 07: SMBus



Libraries

Name						Process Form Fact	
RGO	TSMC07	18V33	7FF	20C	SMB	7FF	Staggered

Summary

The SMBus library provides open-drain bi-directional I/O cells designed for the High-Power SMBus two-line interface. It is compliant with the Rev 3.1 of the SMBus specification.

The design supports the Sm, Fm and Fm+ modes of operation at the SMBus operating voltage (VDDP) of either extended range 3.3V or standard 1.8V logic.

This 7nm library is available in a staggered flip chip implementation.

To utilize these cells in the pad ring, an additional library is required – 1.8V Support: Power. That library contains the power cells, the POC cell, and a rail splitter to isolate the SMBus cells in their own power domain as recommended. It also contains an input-only buffer, isolated analog I/O, and a full complement of power cells along with corner and spacer cells to assemble a complete pad ring by abutment. The rail splitter allows multiple power domains to be isolated in the same pad ring while maintaining continuous VDD/VSS for robust ESD protection.

ESD Protection:

- JEDEC compliant
 - 2KV ESD Human Body Model (HBM)
 - 500 V ESD Charge Device Model (CDM)

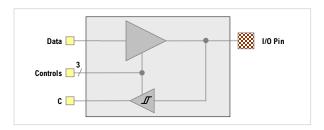
Latch-up Immunity:

- JEDEC compliant
 - Tested to I-Test criteria of ± 100mA @ 125°C

Cell Size & Form Factor

Staggered (pad-limited) – TBDμm x TBDμm

SMP ON 003 1833V NC



Product Features

- Supported I2C operating modes:
 - Standard-mode (Sm) 10 to 100 kbps data rate
 - Fast mode (Fm) 10 to 400 kbps data rate
 - o Fast mode (Fm+) 10 kbps to 1 Mbps data rate
- Open drain operation only (floating NWELL with PMOS used for ESD protection only)
- Built-in output slew rate control to meet I²C T_{of} minimum of (20 x VDDP/5.5V) ns
- Output enable
- Receiver enable
- ESD protection is accomplished with an SCR (no diode to the positive power supply)
- Standard LVCMOS compatible inputs with Schmitt trigger (hysteresis) option
- Power-on sequencing independent design with Power-On Control
- DVDD = 1.62V to 1.98V
- Pad VDDP (power supply reference for Output)
 - 2.7V to 3.63V extended range 3.3V
 - o 1.62V to 1.98V standard range 1.8V
- The circuit consumes no DC supply current in the static state

An open-drain design, this cell requires an external pull-up resistor to a high voltage power supply. The pull-up power supply (VDDP) can be 3.63V maximum, independent of the I/O cell power supply (DVDD). In a 1.8V SMBus application, VDDP can track DVDD but it is not necessary.

Vertical-only (_V) and and horizontal-only (_H) variants provided.

Recommended operating conditions

	Description		Min	Nom	Max	Units
V_{DVDD}	I/O supply voltage		1.62	1.8	1.98	V
V _{VDDP}	External pull-up supply to PAD	3.3V	2.70	3.3	3.63	V
		1,8V	1.62	1.8	1.98	V
V _{VDD}	Core supply voltage		0.675	0.75	0.825	V
			0.765	0.85	0.935	V
TJ	Junction temperature		-40	25	125	°C
V_{PAD}	Voltage at PAD		$V_{\text{DVSS}} - 0.3$	-	3.63	V

Characterization Corners *

Model	LPE Type	VDD [1]	DVDD [2]	Temp
FF	Cbest_CCbest	+10%	+10%	-40°C
FF	Cbest_CCbest	+10%	+10%	125°C
TT	Ctypical	nominal	nominal	25°C
TT	Ctypical	nominal	nominal	85°C
SS	Cworst_CCworst	-10%	-10%	-40°C
SS	Cworst_CCworst	-10%	-10%	125°C

[1] VDD = 0.75V [2] DVDD = 1.8V * PRELIMINARY

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