

TSMC 06/07: 3.3V Support: Power



Libraries

Name	Process	Form Factor
RGO_TSMC06_18V33_6FF_20F_SPT	6FF	Staggered Flip Chip
RGO_TSMC07_18V33_7FF_20C_SPT	7FF	Staggered Flip Chip

Summary

The 3.3V Support: Power library provides a full complement of cells to support the assembly of a functional pad ring by abutment. It is supplied as a standard addition to the GPIO libraries and other I/O library offerings from Aragio Solutions that use a compatible pad ring bus structure.

This library is offered at both 6nm and 7nm. It is available in a staggered flip chip implementation.

The included rail splitter allows multiple power domains to be isolated in the same pad ring while maintaining continuous VDD/VSS for robust ESD protection.

ESD Protection:

- JEDEC compliant
 - 2kV ESD Human Body Model (HBM)
 - 500 V ESD Charge Device Model (CDM)

Latch-up Immunity:

- JEDEC compliant
 - Tested to I-Test criteria of $\pm 100\text{mA}$ @ 125°C

Cell Size & Form Factor

- Staggered (pad-limited) – $34.08\mu\text{m} \times 214.68\mu\text{m}$
- Flip chip implementation with CUP structure built in

Recommended Operating Conditions

Description	Min	Nom	Max	Units
V_{VDD} Core supply voltage	0.675	0.75	0.825	V
	2.97	3.3	3.63	V
	2.25	2.5	2.75	V
V_{DVDD} I/O supply voltage	1.62	1.8	1.98	V
	1.08	1.2	1.32	V
	-40	25	125	$^\circ\text{C}$
T_{J} Junction temperature	-40	25	125	$^\circ\text{C}$
V_{PAD} Voltage at PAD	$V_{\text{DVSS}} - 0.3$	-	$V_{\text{DVDD}} + 0.3$	V

Cell List

Name	Description
Digital Pads	
STP_IN_001_1833V_NC	Input-only buffer
I/O Power / Ground Pads	
PWP_VD_RDO_1833V	I/O power (DVDD)
PWP_VS_RDO_1833V	I/O ground (DVSS)
Core Power / Ground Pads	
PWP_VD_RCD_1033V	Core power (VDD)
PWP_VS_RCD_1033V	Core ground (VSS)
Analog Pads	
ANP_BI_DWR_1833V	Isolated analog input cell
Analog Power / Ground Pads	
PWP_VD_ANA_1033V	Analog power (AVDD) 1.0V
PWP_VS_ANA_1033V	Analog ground (AVSS)
PWP_VD_ANA_1833V	Analog power (ADVDD) 3.3V
PWP_VS_ANA_1833V	Analog ground (ADVSS)
Support Pads	
SPP_CO_000_1833V	Corner cell (rail splitter)
SPP_CO_001_1833V	Corner cell (continuous)
SPP_SP_000_1833V	0.1 μm spacer
SPP_SP_001_1833V	1 μm spacer
SPP_SP_002_1833V	2 μm spacer
SPP_SP_005_1833V	5 μm spacer
SPP_SP_010_1833V	10 μm spacer
SPP_RS_005_1833V	Rail splitter
SPP_RE_SVR_1833V	VREF / HVPS generation
SPP_SP_POC_1833V	POC generation

Characterization Corners

Model [1]	LPE Type	VDD=0.75V	DVDD [2]	Temp
FF	Cbest_CCbest	+10%	+10%	-40 $^\circ\text{C}$
FF	Cbest_CCbest	+10%	+10%	0 $^\circ\text{C}$
FF	Cbest_CCbest	+10%	+10%	125 $^\circ\text{C}$
FFG	Ctypical	+10%	+10%	125 $^\circ\text{C}$
TT	Ctypical	nominal	nominal	25 $^\circ\text{C}$
TT	Ctypical	nominal	nominal	85 $^\circ\text{C}$
SS	Cworst_CCworst	-10%	-10%	-40 $^\circ\text{C}$
SS	Cworst_CCworst	-10%	-10%	0 $^\circ\text{C}$
SS	Cworst_CCworst	-10%	-10%	125 $^\circ\text{C}$

[1] Listed models are for 7FF. 6FF models are FFGNP / TT / SSGNP.
 [2] DVDD = 3.3V, 2.5V, 1.8V & 1.2V

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