

# TSMC 16/12: 3.3V GPIO



## Libraries

Name	Process	Form Factor
RGO_TSMC16_18V33_FFC_20C	FFC	Staggered CUP
RGO_TSMC16_18V33_FFC_45C	FFC	Inline CUP
RGO_TSMC12_18V33_FFC_LL_20C	FFC_LL	Staggered CUP
RGO_TSMC12_18V33_FFC_LL_45C	FFC_LL	Inline CUP

## Summary

The 3.3V GPIO library provides general purpose bidirectional I/O cells. These programmable, multi-voltage I/O's give the system designer the flexibility to design to a wide range of performance targets.

These libraries are offered at both 16nm and a 12nm shrink. They are available in inline and staggered CUP wire bond implementations with a flip chip option.

To design a functional I/O power domain with these cells, an additional library is required – 3.3V Support: Power. That library contains an input-only buffer, isolated analog I/O, and a full complement of power cells along with corner and spacer cells to assemble a complete pad ring by abutment. An included rail splitter allows multiple power domains to be isolated in the same pad ring while maintaining continuous VDD/VSS for robust ESD protection.

### ESD Protection:

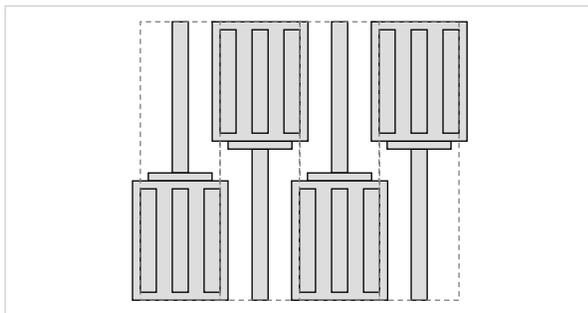
- JEDEC compliant
  - 2KV ESD Human Body Model (HBM)
  - 500 V ESD Charge Device Model (CDM)

### Latch-up Immunity:

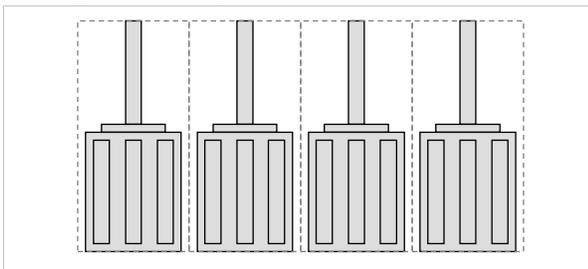
- JEDEC compliant
  - Tested to I-Test criteria of  $\pm 100\text{mA}$  @  $125^\circ\text{C}$

## Cell Size & Form Factor

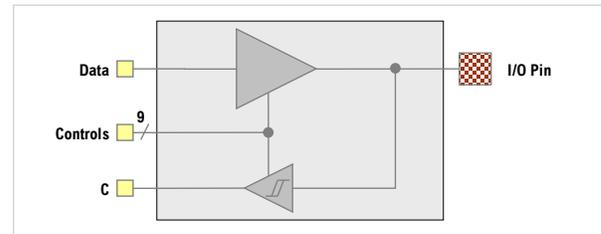
### Staggered (pad-limited) – $32.208\mu\text{m} \times 165.024\mu\text{m}$



### Inline (core-limited) – $45.12\mu\text{m} \times 117.264\mu\text{m}$



## SRP\_BI\_SDS\_1833V\_STB



## Bidirectional GPIO Driver Features

- Multi-Voltage (1.2V, 1.8V, 2.5V, 3.3V)
- LVCMOS / LVTTTL input with selectable hysteresis
- Programmable drive strength (rated 2mA to 12mA)
- Selectable output slew rate
- Optimized for EMC with SSO factor of 8
- Open-drain output mode
- Programmable input options (pull-up/pull-down/repeater)
- Power-On Start (POS) capable
- Power sequencing independent design with Power-On Control

In full-drive mode, this driver can operate to frequencies in excess of 100MHz with 15pF external load and 125 MHz with 10pF load. Actual frequency limits are load and system dependent. A maximum of 200 MHz can be achieved under small capacitive loads.

Vertical-only (\_V) and horizontal-only (\_H) variants provided.

## Recommended operating conditions

Description	Min	Nom	Max	Units
V <sub>VDD</sub> Core supply voltage	0.72	0.80	0.88	V
	2.97	3.3	3.63	V
	2.25	2.5	2.75	V
V <sub>IOVDD</sub> I/O supply voltage	1.62	1.8	1.98	V
	1.08	1.2	1.32	V
	-40	25	125	°C
T <sub>J</sub> Junction temperature				
V <sub>PAD</sub> Voltage at PAD	V <sub>DVSS</sub> -0.3	-	V <sub>DVDD</sub> +0.3	V

## Characterization Corners (16nm)

Model	LPE Type	VDD=0.8V	DVDD [1]	Temp
FFGNP	Cbest_CCbest_T	+10%	+10%	-40°C
FFGNP	Cbest_CCbest_T	+10%	+10%	0°C
FFGNP	Cbest_CCbest_T	+10%	+10%	125°C
FFG	Ctypical	+10%	+10%	125°C
TT	Ctypical	nominal	nominal	25°C
TT	Ctypical	nominal	nominal	85°C
SSGNP	Cworst_CCworst_T	-10%	-10%	-40°C
SSGNP	Cworst_CCworst_T	-10%	-10%	0°C
SSGNP	Cworst_CCworst_T	-10%	-10%	125°C

[1] DVDD = 1.2V, 1.8V, 2.5V & 3.3V

## Characterization Corners (12nm)

Model	LPE Type	VDD=0.8V	DVDD [1]	Temp
FF	Cbest_CCbest	+10%	+10%	-40°C
FF	Cbest_CCbest	+10%	+10%	0°C
FF	Cbest_CCbest	+10%	+10%	125°C
FFG	Ctypical	+10%	+10%	125°C
TT	Ctypical	nominal	nominal	25°C
TT	Ctypical	nominal	nominal	85°C
SS	Cworst_CCworst	-10%	-10%	-40°C
SS	Cworst_CCworst	-10%	-10%	0°C
SS	Cworst_CCworst	-10%	-10%	125°C

[1] DVDD = 1.2V, 1.8V, 2.5V & 3.3V

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