TSMC22: 3.3V Oscillators

Libraries

Name	Process	Form Factor
RGO_TSMC22_18V33_ULP_20C_OSC	ULP	Staggered CUP

Summary

The 3.3V Oscillators library provides oscillator macro cells designed to generate an asynchronous on-chip clock signal with an appropriate external oscillator crystal.

- 32 kHz Real Time Clock Oscillator
- 100 MHz programmable-wide-range oscillator

This library is available in a staggered CUP wire bond implementation with a flip chip option.

To design an operational I/O power domain with these cells, an additional library is required – 3.3V Support: Power. That library contains the CUP / flip chip cells for bonding, DVDD / DVSS power cells, and a full complement of support cells to assemble a functional pad ring by abutment. An included rail splitter allows multiple power domains to be isolated in the same pad ring while maintaining continuous VDD/VSS for robust ESD protection.

ESD Protection:

- JEDEC compliant
  - 2kV ESD Human Body Model (HBM)
  - 500V ESD Charge Device Model (CDM)

Latch-up Immunity:

- JEDEC compliant
  - Tested to I-Test criteria of ± 100mA @ 125°C

Cell Size & Form Factor

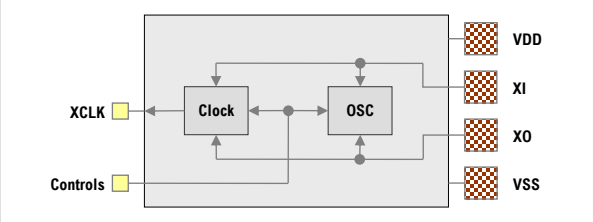
- Staggered (pad-limited)
  - 32kHz Osc – 200µm x 165µm
  - 100MHz Osc – 100µm x 165µm

Recommended Operating Conditions

	Description	Min	Nom	Max	Units
V_{VDD}	Core supply voltage	0.81	0.9	0.99	V
V_{DVDD}	I/O supply voltage	1.62	1.8	1.98	V
		2.25	2.5	2.75	V
		2.97	3.3	3.63	V
T_J	Junction temperature	-40	25	125	°C
V_{PAD}	Voltage at XI [1]	0	-	V_{VDD}	V

[1] XI can be driven by an external clock.
XO should never be driven or loaded by anything other than the crystal.

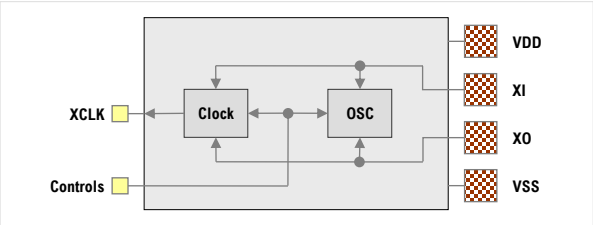
OSP_BI_032_33V



32 KHz RTC Oscillator Features

- Designed to use a 32.768 kHz external crystal
- Optimized for stability, minimum jitter & low power (2.6µW)
- Characterized with crystal loading capacitors ranging from 4 pF to 25 pF.
- Power-down mode
- Bypass mode
- Speed-up circuitry for fast startup
- Operates on core power only (VDD/VSS cells embedded)

OSP_BI_100_33V



100 MHz Programmable Oscillator Features

- Programmable drive strength – wide frequency range
- Low self-noise – optimized for stability and minimum jitter
- Frequency range – ≥ 1 MHz to 100 MHz
- Characterized with industry-standard crystals
- Power-down mode
- Forced bypass mode
- Operates on core power only (VDD/VSS cells embedded)

Characterization Corners

Nom VDD	Model	LPE	VDD	DVDD [1]	Temp
0.9V	FF	Cbest	+10%	+10%	-40°C
	FF	Cbest	+10%	+10%	0°C
	FF	Cbest	+10%	+10%	125°C
	FFG	Ctypical	+10%	+10%	125°C
	TT	Ctypical	nominal	nominal	25°C
	TT	Ctypical	nominal	nominal	85°C
	SS	Cworst	-10%	-10%	-40°C
	SS	Cworst	-10%	-10%	0°C
	SS	Cworst	-10%	-10%	125°C

[1] DVDD = 1.8V, 2.5V, 3.3V

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