TSMC22: (R)GMII

Libraries

Name	Process	Form Factor
RGO_TSMC22_18V33_ULP_20C_RGMII	ULP	Staggered CUP

Summary

The (R)GMII library provides driver / receiver cells for both Gigabit Media Independent Interface signaling and Reduced Gigabit Media Independent Interface signaling. It is designed to interface Ethernet PHY to network switch ASICs. It is compliant with IEEE 802.2-2005 (GMII) and HP RGMII, version 1.3, 12/10/2000.

This library is available in a staggered CUP wire bond implementation with a flip chip option.

To design an operational I/O power domain with these cells, an additional library is required – 3.3V Wide Range GPIO. That library contains a full complement of cells to support the assembly of a functional pad ring by abutment. That set includes an input-only buffer, isolated analog I/O, and power / ground cells along with corner and spacer cells. An included rail splitter allows multiple power domains to be isolated in the same pad ring while maintaining continuous VDD/VSS for robust ESD protection.

ESD Protection:

- JEDEC compliant
  - 2kV ESD Human Body Model (HBM)
  - 500V ESD Charge Device Model (CDM)

Latch-up Immunity:

- JEDEC compliant
  - Tested to I-Test criteria of ± 100mA @ 125°C

Cell Size & Form Factor

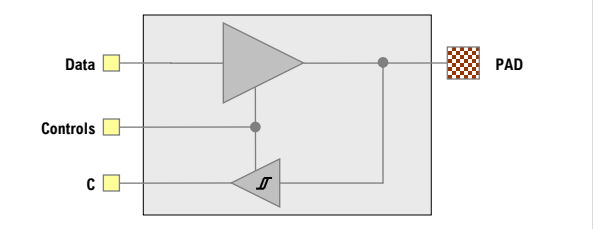
- Staggered (pad-limited)
  - MIP / RIP – 25µm x 165µm
  - VREF – 40µm x 165µm

Characterization Corners

Nom VDD	Model	LPE	VDD	DVDD [1]	Temp
0.9V	FF	Cbest	+10%	+10%	-40°C
	FF	Cbest	+10%	+10%	0°C
	FF	Cbest	+10%	+10%	125°C
	FFG	Ctypical	+10%	+10%	125°C
	TT	Ctypical	nominal	nominal	25°C
	TT	Ctypical	nominal	nominal	85°C
	SS	Cworst	-10%	-10%	-40°C
	SS	Cworst	-10%	-10%	0°C
	SS	Cworst	-10%	-10%	125°C

[1] DVDD = 1.8V, 2.5V, 3.3V

MIP_BI_SDS_1833V_NC & RIP_BI_SDS_1833V_NC



(R)GMII Combo Driver Features:

- 3.3V GMII mode
- 2.5V & 1.8V RGMII modes

RGMII Driver Features:

- 3.3V GMII mode
- 3.3V, 2.5V & 1.8V RGMII modes

For proper operation, the **SPP_RE_MVR_182533V** voltage reference cell, included in this library, is required in the (R)GMII power domain.

Recommended Operating Conditions

	Description		Min	Nom	Max	Units
V_{VDD}	Core supply voltage		0.81	0.9	0.99	V
T_J	Junction temperature		-40	25	+125	°C
V_{PAD}	Voltage at IO		0		V_{DVDD}	V
V_{DVDD}	I/O supply voltage	3.3V GMII / RGMII	2.97	3.3	3.63	V
V_{IH}	Input logic high		1.7	-	-	V
V_{IL}	Input logic low		-	-	0.9	V
V_{IL_AC}	Input high, AC		1.9	-	-	V
V_{IH_AC}	Input low, AC		-	-	0.7	V
V_{OH}	Output logic high		2.1	-	3.6	V
V_{OL}	Output logic low		0	-	0.5	V
V_{DVDD}	I/O supply voltage	2.5V RGMII	2.25	2.5	2.75	V
V_{IH}	Input logic high		1.7	-	-	V
V_{IL}	Input logic low		-	-	0.7	V
V_{OH}	Output logic high		2.0	-	V_{DVDD}+0.3	V
V_{OL}	Output logic low		V_{DVSS}-0.3	-	0.4	V
V_{DVDD}	I/O supply voltage	1.8V RGMII	1.62	1.8	1.98	V
V_{IH}	Input logic high		0.7*V_{DVDD}	-	V_{DVDD}+0.3	V
V_{IL}	Input logic low		V_{DVSS}-0.3	-	0.3*V_{DVDD}	V
V_{OH}	Output logic high @ I_{OH} = 100µA		0.85*V_{DVDD}	-	V_{DVDD}+0.3	V
V_{OL}	Output logic low @ I_{OL} = 100µA		V_{DVSS}-0.3	-	0.15*V_{DVDD}	V
F	Clock frequency / accuracy		2.5[1] - 100ppm		125 + 100ppm	MHz

[1] The lowest supported frequency is 10BASE-T over RGMII

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