TSMC22: 3.3V Support: Power

Libraries

Name	Process	Form Factor
RGO_TSMC22_18V33_ULP_20C_SPT	ULP	Staggered CUP
RGO_TSMC22_18V33_ULL_20C_SPT	ULL	Staggered CUP

Summary

The 3.3V Support: Power library provides a full complement of cells to support the assembly of a functional pad ring by abutment. It is supplied as a standard addition to the GPIO libraries and other I/O library offerings from Aragio Solutions that use a compatible pad ring bus structure.

This library is available in a staggered CUP wire bond implementation with a flip chip option.

The included rail splitter allows multiple power domains to be isolated in the same pad ring while maintaining continuous VDD/VSS for robust ESD protection.

ESD Protection:

- JEDEC compliant
  - 2kV ESD Human Body Model (HBM)
  - 500V ESD Charge Device Model (CDM)

Latch-up Immunity:

- JEDEC compliant
  - Tested to I-Test criteria of ± 100mA @ 125°C

Cell Size & Form Factor

- Staggered (pad-limited) – 25µm x 165µm

Characterization Corners

Nom VDD	Model	LPE	VDD	DVDD [1]	Temp
0.9V	FF	Cbest	+10%	+10%	-40°C
	FF	Cbest	+10%	+10%	0°C
	FF	Cbest	+10%	+10%	125°C
	FFG	Ctypical	+10%	+10%	125°C
	TT	Ctypical	nominal	nominal	25°C
	TT	Ctypical	nominal	nominal	85°C
	SS	Cworst	-10%	-10%	-40°C
	SS	Cworst	-10%	-10%	0°C
	SS	Cworst	-10%	-10%	125°C

[1] DVDD = 1.8V, 2.5V, 3.3V

Support Cells

Name	Description
Digital Pads	
STP_IN_001_33V_NC	Input-only buffer
I/O Power / Ground Pads	
PWP_VD_RDO_33V	I/O power (DVDD)
PWP_VS_RDO_33V	I/O ground (DVSS)
Core Power / Ground Pads	
PWP_VD_RCD_1033V	Core power (VDD)
PWP_VS_RCD_1033V	Core ground (VSS)
Analog Pads	
ANP_BI_DWR_33V	Isolated analog input cell
Analog Power / Ground Pads	
PWP_VD_ANA_1033V	Analog power (AVDD) 1.0V
PWP_VS_ANA_1033V	Analog ground (AVSS)
PWP_VD_ANA_33V	Analog power (ADVDD) 3.3V
PWP_VS_ANA_33V	Analog ground (ADVSS)
Support Pads	
SPP_CO_000_33V	Corner cell (rail splitter)
SPP_CO_001_33V	Corner cell (continuous)
SPP_SP_000_33V	0.1µm spacer
SPP_SP_001_33V	1µm spacer
SPP_SP_002_33V	2µm spacer
SPP_SP_005_33V	5µm spacer
SPP_SP_010_33V	10µm spacer
SPP_RS_005_33V	Rail splitter
SPP_RE_SVR_182533V	VREF generation
SPP_SP_POC_1833V	POC generation

CUP Cells

Staggered CUP Cells	
CUP_TSMC28_40X80_IN	40µm X 80µm inner
CUP_TSMC28_40X80_OUT	40µm X 80µm outer
CUP_TSMC28_44X80_IN	44µm X 80µm inner
CUP_TSMC28_44X80_OUT	44µm X 80µm outer
CUP_TSMC28_48X48_IN	48µm X 48µm inner
CUP_TSMC28_48X48_OUT	48µm X 48µm outer
CUP_TSMC28_33V_FC	Flip-chip cell

Recommended Operating Conditions

	Description	Min	Nom	Max	Units
V_{VDD}	Core supply voltage	0.81	0.9	0.99	V
V_{DVDD}	I/O supply voltage	1.62	1.8	1.98	V
		2.25	2.5	2.75	V
		2.97	3.3	3.63	V
T_J	Junction temperature	-40	25	125	°C
V_{PAD}	Voltage at PAD	V_{DVSS} -0.3	-	V_{DVDD} +0.3	V

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